## 2002 SCHEME

Fifth Semester B.E. Degree Examination, Dec.08/Jan.09	
Fifth Semester B.E. Degree Examinate Linear IC's	
Operational Amplifiers and 2.110 Max. Marks:100	
Note: 1. Answer any FIVE full questions  Note: 1. Answer any FIVE full questions  2. Use of resistor and capacitor standard values list and OP amp data sheets are permitted.  Explain the operation of high input impedance capacitor coupled non-inverting amplifier with a (06 Marks)	
neat circuit diagram.  Cive the description of capacitor coupled non-inverting amplifier using a single polarity supply  (06 Marks)	
A capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a A capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a A capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a load resistance of 4.7ks2 having a capacitor coupled voltage follower is to be designed for a capacit	
Design and draw a suitable circuit.  Discuss the effect of stray Capacitance on an opamp circuit stability. Hence write the equations to determine the value of input stray capacitance that might produce circuit instability. (07 Marks) to determine the value of input stray capacitance that might produce circuit instability. (07 Marks)  Discuss the effects of slew rate on (i) Bandwidth and output amplitude. (ii) Output pulse rise time (07 Marks)	
and amplitude.  Calculate the minimum rise time and the maximum undistorted output pulse amplitude at that  Calculate the minimum rise time and the maximum undistorted output pulse amplitude at that  Calculate the minimum rise time and the maximum undistorted output pulse amplitude at that  Calculate the minimum rise time and the maximum undistorted output pulse amplitude at that  Calculate the minimum rise time and the maximum undistorted output pulse amplitude at that  Calculate the minimum rise time and the maximum undistorted output pulse amplitude at that  Calculate the minimum rise time and the maximum undistorted output pulse amplitude at that  (06 Marks)	
rise time for an amphile with a summing	,
the state of the wave received the state of	,,
• With the aid of a neat circuit diagram and related expression for the holding capacitor and output (06 Marks carrest explain precision peak detector.  • I see pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle peak input voltage of 1V. The listing pipolar opamps design the peak detector circuit to handle p	10
capacitor is to be 5%. Given the discharge current for capacitor I <sub>d</sub> =1 μA (06 Mark	.>)
The form.  (07 Mark)	(s)
C 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	
Specia the circuit of a mangular Rectangular waveform generator and explain the circuit (07 Mari	ks)
Derive as expression for the frequency of oscillations and gain for the Wein bridge oscillate (07 Mar.	ks) put
Line 1: supply of -9V, design a phase shift oscillator to have an out (06 Mar) (10 kHz. Assume current in the feedback path as I <sub>3</sub> =50μA. (06 Mar) (10 kHz. Assume current in the feedback path as I <sub>3</sub> =50μA.	ks)
Expose first order to pass between that what was a second security (06 Mail	rks)
Gree the description of these step filter with the aid of frequency response curve. (06 Mar.  Design a single stage band pass filter to have a voltage gain of 1 and a passband from 300Hz.  (06 Mar.  Hitz selecting C:=1000pF hence sketch the circuit.	z to rks) rks)
Decress the operation of a Voltage tollowed DC voltage regulator. (06 Ma	and
Analyze the circuit to determine the line regulation, load regulation and re-	pple irks)

E explanation to the with relevant circuit diagrams and waveforms wherever applicable: reaction. (20 Marks)

a. Universal active filters

c) Opamp based circuit stability precautions

d) Operation and applications of PLL. Oscillator amplitude stabilization